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09/754,325	01/05/2001	Tomohiro Yamashita	201540US2	3684

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EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N . 09/754,325	Applicant(s) YAMASHITA ET AL.	
	Examiner ori nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 10/25/2002 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

3. Claims 1 and 5-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Wei et al. (5,843,813).

Regarding claim 1, Wei et al. teach in figure 10B and related text (column 10, line 20 to column 11, line 12) a semiconductor device comprising: semiconductor substrate 240;

a first well 274 of a prescribed conductivity type at which a first semiconductor element 246, 278 or 276 is provided, selectively formed in a surface of the semiconductor substrate; a second well 264 of the same conductivity type as the prescribed conductivity type at which a second semiconductor element 268 or 246 is provided, selectively formed in the surface of the semiconductor substrate; a first conductive layer 246 across the first well and the second well in the surface of the semiconductor substrate with an end provided on the first well 274 and another end provided on the second well 264 electrically connecting the first well and the second well, and a first contact 280 electrically connected with the first well 274.

Regarding claim 5, Wei et al. teach in figure 10B and related text (column 10, line 20 to column 11, line 12) a second conductive layer 276 formed in the surface of the semiconductor substrate and provided on the first well 274 without being in contact with the second well 264, wherein the first contact 280 is in contact with the second conductive layer 276.

Regarding claim 6, Wei et al. teach in figure 10B a first conductive layer 246 includes an impurity introduction layer N+ of the same conductivity type as the prescribed conductivity type N. Note that the broad recitation of the claim does not require the first conductive layer to include both an impurity introduction layer of the same conductivity

type as the prescribed conductivity type and a compound layer of the material for the semiconductor substrate and a metal, but only one of an impurity introduction layer of the same conductivity type as the prescribed conductivity type and a compound layer of the material for the semiconductor substrate and a metal.

Regarding claim 7, Wei et al. teach in figure 10B a first conductive layer 246 has lower resistivity (N+) than the first well (N) and the second well (N).

Regarding claim 8, Wei et al. teach in figure 10B a second conductive layer 276 includes an impurity introduction layer N+ of the same conductivity type as the prescribed conductivity type N

Regarding claim 9, Wei et al. teach in figure 10B a second conductive layer 276 has lower resistivity (N+) than the first well (N).

4. Claims 1, 5, 10 and 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Nishigohri (6,384,455).

Regarding claim 1, Nishigohri teaches in figure 16 and related text (column 6, line 61 to column 9, line 10) a semiconductor device comprising: semiconductor substrate 21, first well 41 of a prescribed conductivity type at which a first semiconductor element 32,

36 or 27 is provided, selectively formed in a surface of the semiconductor substrate; a second well 31 (column 9, lines 5-7) of the same conductivity type as the prescribed conductivity type at which a second semiconductor element 35 is provided, selectively formed in the surface of the semiconductor substrate; a first conductive layer 36 (column 9, lines 21-24) across the first well and the second well in the surface of the semiconductor substrate with an end provided on the first well 41 and another end provided on the second well 31 electrically connecting the first well and the second well, and a first contact 38 electrically connected with the first well 41.

Regarding claim 5, Nishigohri teaches in figure 16 and related text (column 6, line 61 to column 9, line 10) a second conductive layer 40 formed in the surface of the semiconductor substrate and provided on the first well 41 without being in contact with the second well 31, wherein the first contact 38 is in contact (electrical contact) with the second conductive layer 40. The broad recitation of the claim does not require the first contact to be in direct contact with the second conductive layer

Regarding the claimed limitations of a second conductive layer formed in the surface of the semiconductor substrate and provided on the first well, a well is a conductive layer, and thus well 40 is a second conductive layer. Nishigohri teaches in figures 17-27 a method of forming the device of figure 16. Region 27 is formed by etching cavity 26 in the substrate (figure 20). The sidewalls of cavity 26 are now the surfaces of the

substrate. Therefore, second conductive layer 40, which is adjacent to the bottom of region 27, is formed in the surface of the semiconductor substrate. Furthermore, Figures 26 and 27 depict the implantation profile of the device, wherein the first and second implantations overlap at their meeting point. Thus, although figure 25 illustrates well 41 and well 40 being adjacent to each other, well 41 and well 40 actually overlap each other. Therefore, the second conductive layer 40 is provided on the first well 41, as claimed.

Regarding claim 10, Nishigohri teaches in figure 16 and related text (column 8, line 63 to column 9, line 4) the first well 41 and the second well 31 have different impurity profiles.

Regarding claim 11, Nishigohri teaches in figure 16 and related text (column 8, line 63 to column 9, line 4) a first semiconductor element being a first MOSFET transistor 33 and a second semiconductor element being a parasitic MOSFET second transistor 21, 41/31, 36 (also see column 3, lines 12 and 21).

Regarding claim 12, Nishigohri teaches in figure 16 a second well 31 being deeper than the first well 41.

Claim Rejections - 35 USC § 102/103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior section.

8. Claims 1-4 and 11 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kikuda et al. (5,519,243). Regarding claim 1, Kikuda et al. teach in figure 3 and related text (column 10, line 20 to column 11, line 12) a semiconductor device comprising: semiconductor substrate 2; a first well 4 of a prescribed conductivity type at which a first semiconductor element 20 is provided formed in a surface of the semiconductor substrate; a second well 33 of the same conductivity type as the prescribed conductivity type at which a second semiconductor element 24 is provided, formed in the surface of the semiconductor substrate; a first conductive layer 6 (a well is a conductive layer) across the first well and the second well in the surface of the semiconductor substrate with an end provided

on the first well 4 and another end provided on the second well 33; and a first contact 280 electrically connected with the first well 274.

Kikuda et al. do not teach selectively forming the first and second wells.

Regarding the limitations of selectively forming the first and second wells, these are process limitations which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 2-4, Kikuda et al. teach in figure 3 a first contact (the right N+ diffusion region) and a second contact 12 being in contact with the first conductive layer 6, wherein the first contact is arranged in opposition to the first well 4 through the

first conductive layer 6 while the second contact 12 is arranged in opposition to the second well 33 through the first conductive layer 6.

Regarding claim 11, Kikuda et al. teach in figure 3 a first semiconductor element being a first MOSFET transistor 20 and a second semiconductor element being a parasitic MOSFET second transistor 24/33, 6, n+ (of transistor 18).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishigohri (6,384,455) in view of Suzuki (6,066,520).

Regarding claim 13, Nishigohri teaches substantially the entire claimed structure, as applied to claim 1 above, except a conductive layer including a compound layer of the material for the substrate and a metal.

Suzuki teaches in figure 1H a conductive layer 125 including a compound layer of the material for the substrate and a metal formed over a conductive layer 123. It would

have been obvious to a person of ordinary skill in the art at the time the invention was made to use a conductive layer including a compound layer of the material for the substrate and a metal in Nishigohri's device in order to reduce the contact resistance of the conductive layer. Note that it is well known in the art to use silicide layer as means to reduce contact resistance.

Regarding claim 14, Nishigohri does not state the conductivity type of the conductive layer. Nishigohri teaches that certain elements such as the substrate can have a P type or N type conductivity (column 7, lines 28-30). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a conductive layer having a conductivity type as that of the first and second wells in Nishigohri's device in order to reduce the contact resistance between the first and second wells and in order not to prevent the transfer of electrons from the first well to the second well in one direction by a P-N junction diode.

11. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei et al. in view of Suzuki (6,066,520).

Regarding claims 13 and 14, Wei et al. teach substantially the entire claimed structure, as applied to claims 1 and 6 above, except a conductive layer including a compound layer of the material for the substrate and a metal.

Suzuki teaches in figure 1H a conductive layer 125 including a compound layer of the material for the substrate and a metal formed over a conductive layer 123. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a conductive layer including a compound layer of the material for the substrate and a metal in Wei et al. 's device in order to reduce the contact resistance between the first well and the second well. Note that it is well known in the art to use silicide layer as means to reduce contact resistance.

Response to Arguments

12. Applicant argues that Wei et al. do not teach first and second semiconductor elements formed in first and second wells.

Wei et al. teach in figure 10B a first well 274 at which a first semiconductor element 246, 278 or 276 is provided, and a second well 264 at which a second semiconductor element 268 or 246 is provided. A semiconductor element can be any element which is used in a semiconductor device. Therefore, FOX regions 268, 278 and doped regions 246, 276 are semiconductor elements.

13. Applicant argues that Kikuda et al. teach wells 4 and 33 are electrically separated from each other, and there is no reason to connect them with well 6.

Kikuda et al. teach wells 4 and 33 are electrically connected to each other with well 6.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Ori Nadav

December 4, 2002